REMARKS/ARGUMENTS

This Amendment is filed with a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. This Amendment is submitted in response to the final Office action of December 30, 2003. Claims 5-7 were previously allowed. Claims 1 and 3-7 are now amended. Claim 8 has been added. Claims 1-8 are pending in the application. Applicant thanks the Examiner for attending to the application.

On page 2 of the action, claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,337,582 issued to Yoshioka. Claim 1 as amended recites "the static driver including a PMOS transistor and an NMOS transistor which are coupled in series between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal…."

Yoshioka does not disclose or suggest a "static driver including a PMOS transistor and an NMOS transistor coupled in series between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal" as recited in amended claim 1. In Yoshioka, as illustrated in driver stages 6, 8, 10 of FIG. 6, a PMOS transistor and an NMOS transistor are coupled in series between a power supply and ground with an output between the PMOS transistor and the NMOS transistor.

The Response to Arguments section of the Office action indicates that "the voltage swing level change from ground level to $V_{dd} - V_{th}$, V_{th} to V_{dd}, or V_{th} to $V_{dd} - V_{th}$... are not stated in the claims 1, 3, and 4." See action, pgs. 3-4. However, it is evident that when a PMOS transistor and an NMOS transistor are coupled in series between a power supply and an output terminal,

the voltage swing level may change from ground level to $V_{dd} - V_{th}$. See, e.g., specification as filed, p. 14, lines 25-29, and FIG. 7. Similarly, when a PMOS transistor and an NMOS transistor are coupled in series between the ground and the output terminal, the voltage swing level may change from V_{th} to V_{dd}. See, e.g., specification as filed, p. 14, lines 29-32, and FIG. 8. When a PMOS transistor and an NMOS transistor are coupled in series between a power supply and an output terminal and between a ground and the output terminal, the voltage swing level may change from V_{th} to $V_{dd} - V_{th}$. See, e.g., specification as filed, p. 14, lines 32-35, and FIG. 9.

On the other hand, the output voltage of Yoshioka becomes V_{cc} or the ground level, and thus cannot realize the reduced output voltage swing from ground to $V_{dd} - V_{th}$ or from V_{th} to V_{dd} as in the present invention.

Accordingly, claim 1 appears to be allowable over Yoshioka. In addition, claims 2 and 3, depending on claim 1, also therefore appear allowable over Yoshioka.

In addition, claim 1 is also amended to correct typographical errors and/or to further avoid suggestion of invocation of 35 U.S.C. §112(6) through use of possible "means-plus-function" language.

Claim 4 is also rejected over Yoshioka. Claim 4 as amended recites "the static driver including a PMOS transistor and an NMOS transistor which are coupled in series between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal…."

As discussed above, Yoshioka does not disclose or suggest a "static driver including a PMOS transistor and an NMOS

transistor coupled in series between at least one of (i) a power supply and an output terminal and (ii) a ground and the output terminal" as recited in amended claim 4, or any resultant reduced voltage swing. Instead, in Yoshioka, as illustrated in driver stages 6, 8, 10 of FIG. 6, a PMOS transistor and an NMOS transistor are coupled in series between a power supply and ground with an output between the PMOS transistor and the NMOS transistor. Accordingly, claim 4 appears to be allowable over Yoshioka.

In addition, claim 4 is also amended to correct typographical errors and/or to further avoid suggestion of invocation of 35 U.S.C. §112(6) through use of possible "means-plus-function" language.

Pg. 4 of the action indicates that claims 5-7 are allowable. Claims 5-7 are now amended for clarity and to further avoid suggestion of invocation of 35 U.S.C. §112(6) through use of possible "means-plus-function" language. Thus, the scope of the coverage provided by these amended claims is believed to remain the same as the previously allowed claims.

New independent claim 8 recites a static driver comprising "a PMOS transistor and an NMOS transistor, a voltage swing level of the static driver changes in at least one of (i) from ground level to V_{dd} - V_{th} and (ii) from V_{th} to V_{dd}, V_{dd} denoting a supply voltage and V_{th} denoting a threshold voltage of the NMOS transistor...." Claim 8, which includes no new matter, is based generally on claim 1 and positively recites aspects of the features of the present invention indicated in the Response to Arguments section of the Office action. See action, pgs. 3-4.

In view of the comments above, it is believed that claim 8 is also allowable in view of Yoshioka.

The application is now in condition for allowance. Accordingly, reconsideration of the application and allowance of claims 1-8 are respectfully requested.

Respectfully submitted,

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